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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: RIEMENS Serial No.: 09/920,042 Filed: 08/01/2001 Title: PROGRAMMED STALL CYCLES SLOW-DOWN VIDEO PROCESSOR	Group Art Unit: 2676 Examiner: Quillen, Allen Docket: PHIL-P008 (NL010506) CERTIFICATE OF MAILING I hereby certify that this correspondence is being deposited with the US Postal Service as First Class Mail in a postage-paid envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313 on April 9, 2004. Signed: Sandra Halliwell Sandra Halliwell

APPEAL BRIEF

Commissioner for Patents

Dear Sir:

In response to the Final Office Action mailed November 24, 2003, Applicant submitted a Notice of Appeal on February 24, 2004. The following Appeal Brief is submitted within the statutory time of Two Months from the Notice of Appeal along with the required fee of $330.

REAL PARTY IN INTEREST

Koninklijke Philips Electronics N.V. is the assignee of the subject patent application.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-8 were finally rejected in Paper 8 mailed November 24, 2003.

STATUS OF AMENDMENTS

Claims 1-8 were filed in the original application. An Amendment was filed June 25, 2003 amending claim 6. An Amendment After Final was submitted on February 24, 2004 and an Advisory Action was mailed on February 25. No Amendments are pending.

SUMMARY OF INVENTION

The invention is directed to reducing bus contention in a video processor. A processor executes image processing under control of a clock facility, such that a sequence of C effective clock cycles will effect a processing operation of a predetermined amount of image information. In particular, the processor has programming means for implementing programmable stall clock cycles interspersed between the effective clock cycles for implementing a programmable slowdown factor S, such that a modified number of C*S overall clock cycles will effect processing of the predetermined amount of image information.

ISSUES

1. Whether the Examiner has met the burden of proving that claims 1-3 and 6 are anticipated by Taraci (USP 6,316,974).
2. Whether the Examiner has met the burden of proving that claims 4, 5, and 8 are obvious in view of Taraci and Crump (USP 5,638,531).
3. Whether the Examiner has met the burden of proving that claim 7 is obvious in view of Taraci and Kondoh (USP 5,649,119).

GROUPING OF CLAIMS

1. Claims 1-3 and 6 stand or fall together.
2. Claims 4, 5 and 8 stand or fall together.
3. Claim 7 stands alone.

ARGUMENT

In the Office Action dated November 24, 2003, claims 1-3 and 6 were rejected under 35 USC §102 in view of Taraci. Claims 4, 5 and 8 were rejected under §103 in view of Taraci and Crump. Claim 7 was rejected under §103 in view of Taraci and Kondoh.

Prior Art Rejections

A rejection under 35 USC §102 requires that the cited reference teach all the claimed elements. A rejection under 35 USC §103 requires that the combined references suggest the claimed combination. (MPEP 706 and 2141 et seq.).

Under the Graham test, three factors must be evaluated: the scope and content of the prior art; the differences between the prior art and the claimed invention; and the level or ordinary skill in the art. (MPEP 706 and 2141 et seq.).

GROUP 1 (35 USC §102)

Claims 1-3 and 6 were rejected under 35 USC §102 in view of Taraci. In order to serve as a §102 reference, the reference must teach all the claimed elements.

Claim 1 is directed to a processor for executing image processing "being characterized in having programming means for implementing programmable stall clock cycles . . ." The patent specification describes an exemplary "means" for implementing the function as an accumulator (see Specification page 4 lines 21-28 and Fig. 4). The invention exemplary embodiment employs the carry output as the effective clock. This creates the programmable stall clock function.

Taraci is directed to a technique for synchronizing video inputs to a particular output. Taraci does not teach a programmable stall clock, but rather a synchronization technique. The Examiner cites a portion of the reference (col. 8 lines 35-50) and contends that Taraci describes a frame rate delay equivalent to the claimed programmable stall clock.

The Taraci reference is directed to very different problem than in the subject Application. Taraci intends to synchronize inputs and outputs, while the subject Application is directed to reducing video processor bus contention by applying a programmable stall clock. Consequently, Applicant submits that the Taraci structure and function is for video synchronization, not for implementing a programmable stall clock. Applicant strenuously disagrees that the Taraci frame rate delay is the same as the claimed programmable stall clock.

Accordingly, Applicant submits that the Taraci reference does not teach all the claimed elements, and therefore, cannot serve as a §102 reference to reject claims 1-3 and 6.

GROUPS 2 AND 3 (35 USC §103)

Claims 4, 5 and 8 were rejected under §103 in view of Taraci and Crump. Claim 7 was rejected under §103 in view of Taraci and Kondoh.

As described above, Applicant submits that claim 1 is allowable over the Taraci reference. Accordingly, Applicant submits that the dependent claims 4, 5, 7 and 8 are also allowable.

The Taraci reference is directed to synchronizing video inputs and outputs, while the subject Application is directed to reducing video processor bus contention. Consequently, Applicant submits that the Taraci structure and function is for video synchronization, not for implementing a programmable stall clock. Applicant strenuously disagrees that the Taraci frame rate delay is the same as the claimed programmable stall clock.

The Crump reference is directed to video refresh technique that reduces complications between different video formats.

The Kondoh reference is directed to a technique for data queuing. Neither of these references teaches or suggests a programmable stall clock.

Under the Graham analysis, the scope and content of the Taraci reference is different than the presently claimed invention, and there are significant differences between the Taraci reference and the presently claimed invention. Finally, there is simply no suggestion in the references to combine them in a manner that would result in the presently claimed invention.

Accordingly, Applicant submits that the Taraci reference in combination with the Crump or Kondoh references does not teach or suggest the claimed invention, and therefore, cannot serve as §103 references to reject claims 4, 5, 7 and 8.

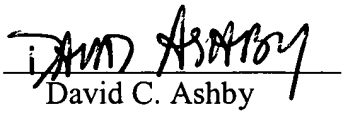
CONCLUSION

For the reasons set forth above, Applicant requests that the Board overturn the Examiner's rejections and pass the claims to issue.

If any matters can be resolved by telephone, Applicant requests that the Patent and Trademark Office call the Applicant at the telephone number listed below.

Respectfully submitted,

IP Strategy Group (IPSG, P.C.)
10121 Miller Ave, Suite 201
Cupertino, CA 95014
Tel: 408-257-5500
Fax: 408-257-5550

By: 
David C. Ashby
Reg. No. 36,432

APPENDIX

PENDING CLAIMS

1. (Original) A processor for executing image processing under control of a clock facility, such that a sequence of C effective clock cycles will effect a processing operation of a predetermined amount of image information, said processor being characterized in having programming means for implementing programmable stall clock cycles interspersed between said effective clock cycles for implementing a programmable slowdown factor S, such that a modified number of C*S overall clock cycles will effect processing of said predetermined amount of image information.

2. (Original) A processor as claimed in claim 1, and having said programming means controlling the interspersing in an at least substantially periodical manner.

3. (Original) A processor as claimed in claim 1, effectively representing a coprocessor and having a control processor as said programming means.

4. (Original) A processor as claimed in claim 3, wherein said coprocessor and said control processor are interconnected by a bus to a shared memory facility.

5. (Original) A processor as claimed in claim 4, wherein said coprocessor, said control processor and said bus are disposed on a single semiconductor chip, whereas said shared memory facility is at least substantially off-chip.

6. (Previously Amended) A processor as claimed in claim 1, and being arranged to execute at least two different image processing operations under respective different percentages of stall clock cycles.

7 (Original) A processor as claimed in claim 1, wherein said programming means drive an incrementable storage facility through a periodical increment by a number N that is a function of said factor S according to N=round (R*x, wherein x=(S-1/S) and R is the range of the storage facility, and wherein a carry output signal of the storage facility will generate an effective clock

cycle.

8. (original) A processor as claimed in claim 5, wherein at least one other bus station than the coprocessor is arranged and allowed to temporarily grab the bus in an interval during a said stall cycle.